PROJECT

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for

HIGH-SPEED DATA PROCESSOR SYSTEM RESEARCH

Project LIGHTNING

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Prepared by
Engineering Department
Electronic Data Processing Division
Industrial Electronic Products
RADIO CORPORATION OF AMERICA
Camden, New Jersey

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Chapter 1 GENERAL

1-1. INTRODUCTION

During this quarter, combination of the Logic and the Memory Subsystems was effected and the resulting unified subsystem was operated.

Specifically:

1. Combination

   Several unanticipated problems were recognized and corrected.

   (a) The electrical grounds used by each subsystem were not common, resulting in a 60-cycle circulating current.

   (b) The known incompatibility of design between the two subsystems was further eliminated resulting in several major decisions concerning future work.

   (c) Memory fabrication techniques did not allow for accessibility to the lower planes which contributed much to redesign requirements.

   (d) The two subsystems worked together with the memory operating at a 33-megacycle repetition rate.

2. Extensibility

   The 24-bit word line was operated for long periods of time; no difficulties were encountered.

1-2. INTERPRETIVE SUMMARY

The ultimate goal of this project is the construction and operation of a combined Logic-Memory Subsystem. At the end of this period, the Logic and Memory Subsystems were operated successfully in combination.

A. LOGIC SUBSYSTEM

The Logic Subsystem has been in complete operation for a total of 720 hours. During this period, the total number of failures encountered were 52 of which the largest number were due to solder connections, followed by diode failures and, third, resistors. Nearly all of the failures encountered were catastrophic as opposed to drift, which gives further emphasis to the validity of the mathematical model used in the worst-case design calculations.

B. MEMORY

Although memory performance has not been entirely satisfactory from the reliability point of view, its performance has indicated that the electrical design is satisfactory and all of the basic circuits are proven. The 33-megacycle repetition rate reported at the end of last quarter remains unchanged. Several problems uncovered during this quarter were defined and solved. Examples of these were house grounds and timing generator distribution problems.

The 24-bit extensibility word was operated with repetition rates of up to 65 megacycles, and it performed reliably.

C. COMBINATION

The combined Logic and Memory Subsystem showed up several problems not previously anticipated. Examples of these are:

(1) Hum problems associated with separate ground of the two systems

(2) Some various incompatibilities of pulse amplitudes,

(3) Some timing problems.

These were corrected and the unified subsystem was operated with most of the memory word locations functioning under control of the Logic Subsystem.

This phase of the development has pointed up or re-emphasized the importance of several incompatibilities:

(1) The fabrication scheme used in the memory stack is quite inadequate, and must be redone in its entirety.

(2) The importance of two incompatibilities between logic and memory, previously recognized, were again re-emphasized. These are: the negative polarity of

the standard memory control pulse and the synchronous nature of the memory. The first is considered a relatively minor design to correct, and it is highly desirable that the memory clock pulse be operated upon demand of logic so that the timing situation is under better control.

The aforementioned corrections should be made as soon as possible and the fabrication scheme for memory should be redone likewise. At the completion of these tasks, the memory should operate satisfactorily.

Chapter 2 COMBINATION

Chapter 2 COMBINATION

I. PERSONNEL

The following personnel contributed to this phase of the project during the fifteenth quarter:

G. J. Ammon
L. Dillon
M. M. Kaufman
J. P. McAllister
J. L. Miller
P. Palamar
J. Schopp

II. DISCUSSION

A. REVIEW

1. Memory Subsystem

a. Operating Time Breakdown

The Memory Subsystem, assembled in the main frame, has been in the process of being debugged and has been under test for 710 hours. This time was read from a running time meter coupled to the subsystem's a-c power.

An approximate breakdown of the running time is:

96 hours spent debugging the decoder and word drivers.

168 hours spent debugging the memory stack and regeneration circuits.

320 hours spent installing and debugging combination circuits.

30 hours spent in demonstration.

96 hours spent testing the overall system with carefully established test routines.

b. Memory Reliability

The storage was periodically checked. There were approximately 30 observations made, and during 25, all bits were operating in the write-all-ones or all-zero mode. One bit in the bottom half of the stack stopped operating for the last five

observations. (Observations are taken every three days.) This lack of operation was attributed to a contact resistance increase in the memory cell holder. An attempt to decrease the contact resistance by applying wiper action to the rectifier pushed the rectifier out of the holder. This cell is at the bottom of the stack and therefore no attempt was made to replace it.

A running log of conditions encountered each day of testing and debugging has been kept. A review of this log is shown in Table 2-1 below.

TABLE 2-1
SUMMARY OF AUGUST LOG FOR MEMORY SUBSYSTEM

	Totals
Hours Run	157
Diode Failures	6
Resistor and Contact-Resistance Failures	5
Drift Failures	17
Noise and Grounding Difficulties	5 days
Loose Wafers	8

The noise related to grounding was essentially removed after the system's grounding scheme was detailed on paper and the system was modified. These modifications, which eliminated all detectable 60-cycle hum on the grounds, were as follows: All memory subsystem power supply chassis grounds were disconnected from the circuit grounds. Only one connection to the main house ground in the combined system now exists and that is at the logic subsystem. The only ground connection between the logic subsystem circuits and memory subsystem circuits occurs through their signal interconnection. The house ground and circuit ground are joined only in one place in the combination, at the logic subsystem power supply.

A review of the Memory Subsystem's status is shown in Table 2-2 below:

TABLE 2-2
OPERATING STATUS OF MEMORY SUBSYSTEM

	Present	Goal
Repetition Rate	33 mc (Max)	40 mc
Decode Time	35 ns (Max)	10 ns
Access Time	13 ns (Max)	10 ns
Words Operating (All Modes - With Logic)	22	32
Reliability	Poor	Good

The repetition rate limitation shown in Table 2-2 is primarily a result of the 35-nanosecond decode time. This decode time is based on decoding to one out of 1024 and is for a small 32-word B-box memory using 40-gate subsystem circuits. The decode time can be within the 10-nanosecond goal. Some circuits which are repetition-rate limited at 40 mc could provide 40-mc operation if redesigned to use tunnel resistors for biasing elements.

The 32-word memory, which was built to simulate a 1024-word memory, has proven to be primarily an experimental model with limited worth for observing overall system reliability. It is believed however, that sufficient proof has been given of system and circuit concept feasibility so that a small reliable hardware prototype could be built within a few months. A prototype could be built and tested to indicate the total reliability required to advance to hardware construction.

At the outset of the subsystem construction (Phase III-B), the memory effort required early finalization in four basic areas: memory circuits; logic gates for memory; fabrication techniques; and system organization. It became apparent during the initial test phases that many areas finalized were not compatible. The memory, including concepts and circuits, was under constant change and became basically an experimental model.

The fabrication technique, which was de-emphasized at the outset of the program, represents the area of greatest weakness at the present time. The reliability associated with the experimental model is limited because of the many modifications required. The reliability is also poor because of the basic fabrication techniques used. The memory is constructed so that most of the stack and immediate peripheral equipment are not accessible. It takes approximately one week to disassemble any portion of the stack and immediate peripheral circuitry to correct any failure. This has resulted in reluctancy in repairing any difficulty in and around the stack. There have been device and connector contact-resistance drifts in circuits attributed to the use of conductive epoxy, and some unstable GaAs rectifiers. These changes have been met by shifting nominal bias voltages as opposed to going into the stack and making the required modifications. The overall result has been a decrease in reliability.

Another weak area in the subsystem is associated with the logic gates developed for memory. For example, the inhibit gate requires a drive on a sense amplifier stage which is sufficiently sensitive, under certain conditions, to trigger on the inhibit drive trailing edge. This difficulty resulted in a tightening of tolerances which has added to the poor reliability. There are also read and write registers built on an expediency basis which have more components than necessary. Also voltage and bias relationships exist that are barely compatible with the remaining subsystem.

The subsystem's organization was established at the outset and the "1" outputs from memory are opposite in polarity to the "1" outputs of logic circuitry. This requires inverters which are designed especially for this application.

The timing relationship between logic and memory, with memory operating synchronously and logic operating asynchronously, proved recently to be in error because all conditions were not originally considered. The overall effect however, was aggravation of the present reliability.

It is believed that the memory subsystem as an experimental model with multiple modifications has proven the feasibility of the basic techniques and circuits. There is a sufficient portion of the memory operating properly and reliably so that a hardware prototype can now be built.

c. Redesign

The following steps are needed in the next six months to result in a small design prototype having the reliability required to extrapolate larger production type hardware.

Redevelopment of fabrication techniques is of prime importance. The size of the future tunnel diode memories being considered indicates that the techniques developed for the logic circuits are sufficient for the memory circuits. This represents a departure from the original concept but is proving to be one of the most significant steps recently taken in memory development.

The entire tunnel diode memory is now planned to be built in two wafer frames with memory cells and peripheral circuits constructed on wafers.

A wafer layout for one-half of a 12-bit word is shown in Figure 2-1. This wafer is now in the process of being built and will soon be under test. The wafer also indicates another step related to devices to increase the reliability of the tunnel diode memory. Since the GaAs tunnel rectifiers used for memory do not operate within specification, these may be replaced by two germanium rectifiers. The supply of germanium rectifiers are presently within the required tight tolerances for memory application. The positioning of the components for each memory cell can be seen in Figure 2-1. These components are two germanium rectifiers, one germanium tunnel diode and one resistor. This layout is such that the word line impedance of 10 ohms per 12-bit word is maintained across the wafer. Wafer frames have been built for the logic subsystem, as transmission line structures with extruded copper transmission lines. The memory will maintain that structure. The extruded copper transmission lines have been made between 3.5 ohms and 50 ohms which includes the values required for memory.

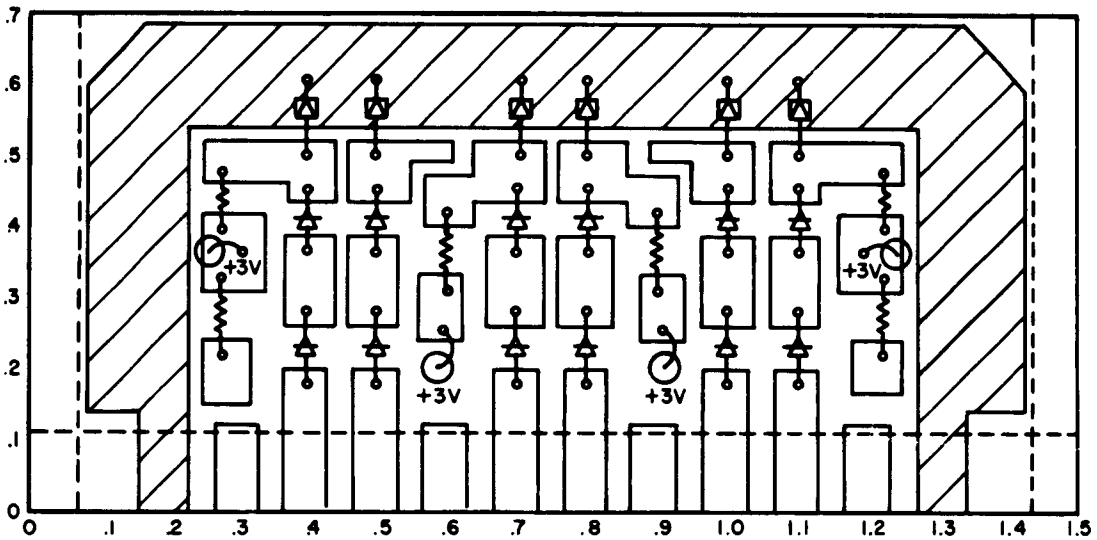


Figure 2-1. Memory Word Wafer

The next area considered for redesign is the logic gates and the system and associated timing relationships.

The present subsystem is controlled by a synchronous generator which produces 18 logic pulses. The redesign would place the memory control in a logic circuit control unit. The memory would then operate asynchronously by an input into the logic unit which would initiate the required logic pulse output.

The logic gates used in a redesign would consist entirely of those gates used in the 40-gate subsystem. The only memory circuits required to be finalized would be the line drivers and sense amplifiers. The timing of the memory would be relaxed by incorporating a dummy digit line (used during a clear-write cycle) to initiate the write drive on the digit line with respect to the read-drive on the word line. The read-drive on the word line would be sensed by the dummy digit line, which after sensing the word line drive would fan-out and clock all digit drivers at the appropriate time. The dummy digit line and related circuits are shown in Figure 2-2. Table 2-3 lists all the areas which would be considered in a redesign.

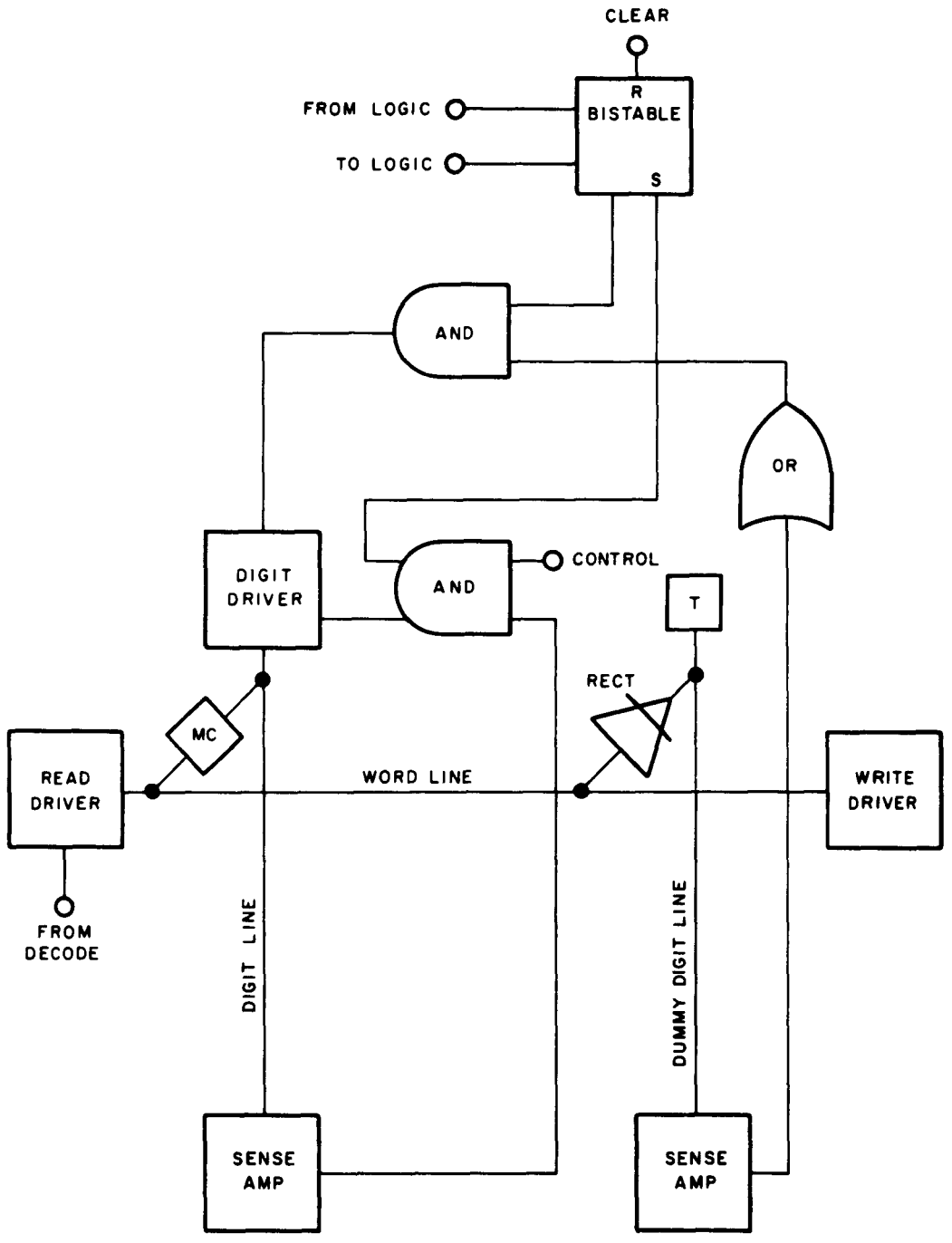


Figure 2-2. Memory Word with Dummy Digit Line

TABLE 2-3
REDESIGN AREAS

Area	Required for Improved Operation
Word Switch and Switch Matrix	Use of Ge TD in place of GaAs TD
Word Read and Write Drivers	Use of TR Biasing Element in place of Resistor Voltage Biasing
TD-TR Memory Cell	Use of 2 Ge TR's in place of GaAs TR.
Digit Driver	Use of TR Biasing Elements in place of Resistor - Voltage Biasing Use of Ge TD's in place of GaAs TD's in all but Output Stage.
Sense Amplifier	Elimination of Sense Amplifier Inhibit Stages and use of AND Gate.
Synchronous Control Generator	Use of Asynchronous Logic Circuit Control
Decoder for One-Out-of-1, 024 Word Memory	Use of 40-Gate Subsystem Circuits for B-Box Memory Decoder
Peripheral Circuits	Use of Logic Circuit Fabrication Techniques for B-Box Memory Use of 40-Gate Subsystem Circuits for all Memory Logic Functions

2. Logic Subsystem

a. Logic Reliability

The Logic Subsystem has been in operation for a total of 720 hours. This is an additional 405 hours beyond the 315 hours reported in IRR-14A. During the past three months there have been 27 failures of the type shown in Table 2-4. This brings the total number of failures to 25 solder connections, 22 diodes, and 5 resistors or a total of 52 during the 720 hours of operation. The times and number of repairs do not include the individual frame debugging cycle before assembly of the logic frames into the main frame. Complete operation of the subsystem in all modes was achieved at 113 hours of operation.

TABLE 2-4
LOGIC SUBSYSTEM FAILURES

	Solder	Diodes	Resistors
Up to 5/21	12	11	2
5/21 - 8/21	13	11	3
TOTALS	25	22	5

It is obvious from the results thus far that solder joints and diodes are the areas of greatest unreliability. Further inspection shows that the major portion of failures are occurring in the two control units and parity check unit #2. These were the first three units constructed. Figure 2-3 shows the number of failures during the period 5/21/62 to 8/21/62 plotted vs. time of wafer completion (the time when all wafers for that particular frame had been constructed and tested). There seems to be a definite break at December, or between the parity check #2 and #1 frames. This becomes more significant when the number of wafers in each frame are considered. The A and X registers are the largest frames, with 66 and 52 wafers, respectively. Next comes control #2 with 32 wafers, control #1 and parity check #1 with 28 each, parity check #2 with 24 and the error counter with 23.

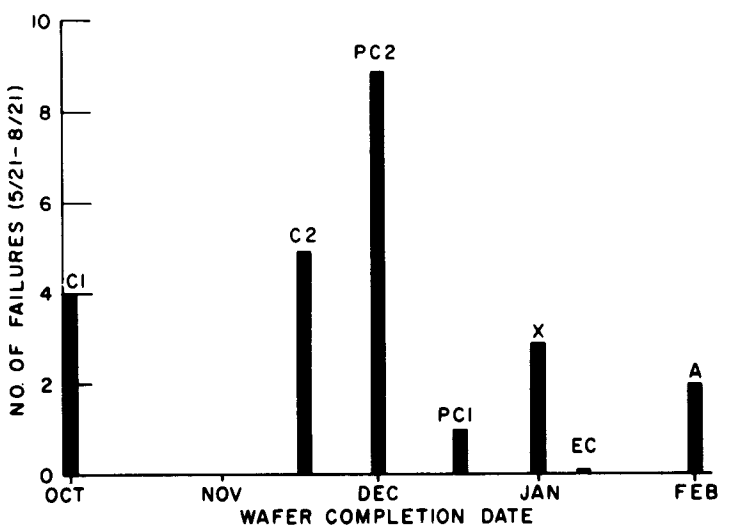


Figure 2-3. Logic Subsystem Failures

Early in the program of subsystem construction, it was required that all OR rectifiers have a capacitance of 1.0 pf or less. This limit was subsequently changed to 1.5 pf due to the very low yield and fragile junctions which resulted from the 1.0 pf limit. This, then, is a possible answer to the situation since 8 of the 11 diode failures were of OR rectifiers.

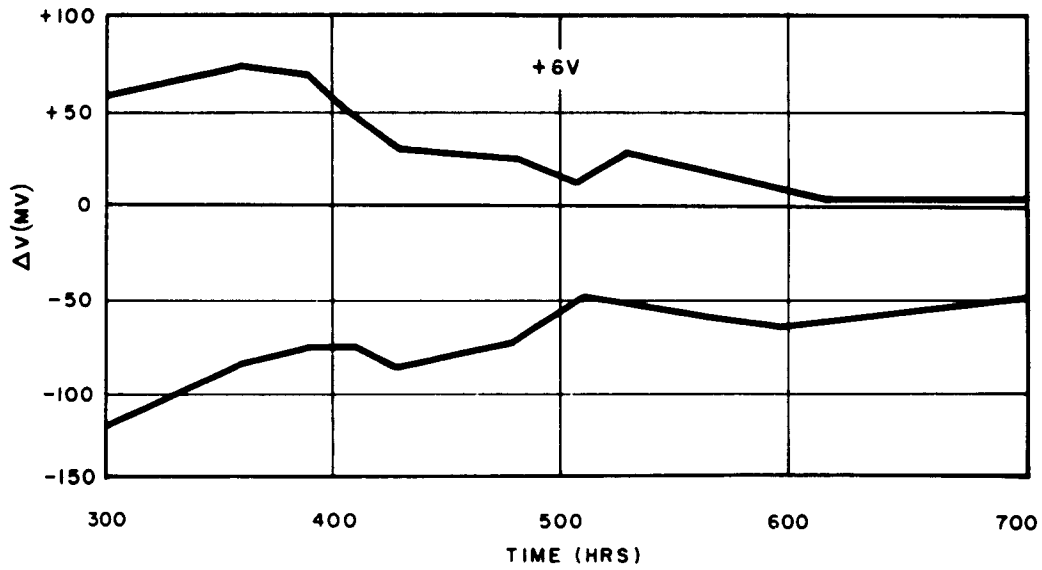
These units have been in operation for a longer period, but a life test of 200 hours was run on the error counter before assembly into the main frame and no failures were recorded in this unit during the period under consideration.

The limit tests on current and voltage biases were conducted during this period and the results of these tests can be seen in Figure 2-4. The read-write registers were connected to the logic at approximately 400 hours and there was a definite drop in operating range after this combination. A series of defects were corrected at the 530-hour mark which opened the limits. However a regular deterioration has occurred, especially in the +6 volt range, during the next 170 hours causing very tight limits at the 700-hour mark. Very little so-called preventive maintenance has been carried on during this period. First it was noted that most of the failures have been catastrophic (a device or solder joint opens suddenly causing completely unreliable operation). Another problem in applying preventive maintenance to the Logic Subsystem is the difficulty in making repairs to the "soldered in" wafers. So much care must be taken, that after 3 to 4 corrections on a wafer, it reaches the point of becoming unrepairable.

Another interesting fact is that no measurable change in the overall delay times can be detected during operation. This would seem to indicate that a marginal test involving increased clock speed would not be too successful.

b. Combination Phase

Combination of logic and memory has been progressing since last quarter. The read-write register was combined with logic at the 400-hour point. Next, the read-write register and logic subsystem was moved to the memory table and physically connected into the sense-amplifier-digit driver loop. This proved to be a little trying on the logic as 17 of 25 failures occurred after this move, even though it was done at approximately the one-half-time point. The combination was then tested from the logic point of view by placing information into the X register and transferring it to the digit drivers via the write register. In the same cycle, by inhibiting the memory sense amplifiers, it was possible to transfer the information to the read register and back to the X register on the memory read command. This process then, made it possible to check out the X$\longrightarrow$WR$\longrightarrow$DD$\longrightarrow$RD$\longrightarrow$X loop. This was done on a one-shot basis with an S.K.L. and at high speed. One difficulty was encountered because 3-foot cables were used on a transfer path between logic and memory to provide room (at least temporarily) to work between the two tables. This caused a timing problem because the write to digit driver clock pulse was occurring before the X$\longrightarrow$WR transfer was complete. This situation was quickly corrected and the transfer loop was checked out.



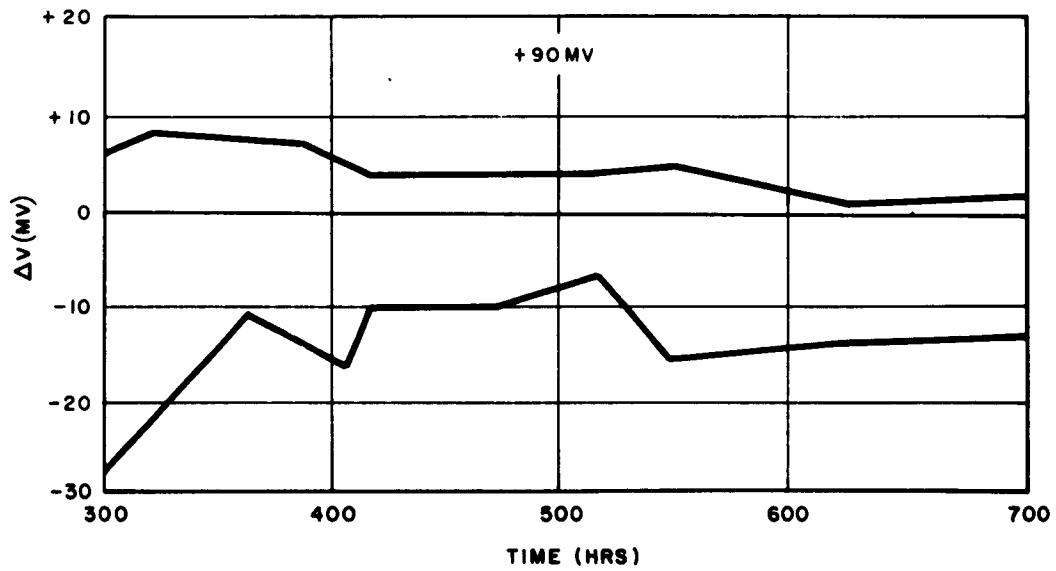


Figure 2-4. Bias Voltage Limits

The next step in combining the logic and memory was to inhibit the sense amplifiers and write into a memory location, then read out of that location. The first attempt at this was successful. However, there was a word in memory which had a bit removed and it produced no parity errors. Upon investigation, it was found that the logic was writing and reading on one memory cycle such that the only thing that was being tested was the X⟶WR⟶DD⟶RR⟶X loop. The memory was being ignored altogether. The solution to this problem is discussed in more detail in Section B: Combination of Logic and Memory Subsystems - Timing and System Checkout.

In the original timing, the write occurred at 16 ns followed by the ISA⟶M and CLRR. The WR⟶DD then occurred which transferred the word to memory since the ISA is on; but also since the same digit driver serves both the memory and the read register, the word also ends up in the read register. It was thought that by the time the RD occurred the logic would not be ready, so this would be ignored and the read would occur on the following memory cycle. Unfortunately, the RD enable in logic occurred before the RD pulse from memory. Thus, the information which was just placed in the read register was placed back in the X register. This could be corrected by adding a delay wafer to the logic and revising the wiring. Due to the complications this might cause, this approach was not taken. Another solution would be to inhibit the RD pulse any time that the inhibit sense amplifier signal is on, since this could be done in a plug-in frame. This approach was discarded because the theoretical fan-out of some circuits would be exceeded.

The solution finally chosen was in the form of a timing change as shown by the timing diagram in Figure 2-5. On the first memory cycle the logic has a "Read Enable". Therefore the word A in the read register is transferred to the X register and the logic goes through its operation. Approximately 4 memory cycles occur during this time at the end of which a "Write Enable" occurs which transfers A+1⟶WR. This is followed by a read which takes the information "B" in the RR and places it in the X register. Then ISA is turned on, the WR⟶DD occurs and A+1 is written into memory.

In this manner then, two groups of data are exchanged between logic and memory. This is a much better test of the memory for the system as it is not restricted to a set sequential pattern but can handle two unrelated data words. This operation has been checked out in 22 word locations and is running at full memory and logic speed.

B. COMBINATION OF LOGIC AND MEMORY SUBSYSTEM

1. Timing and System Checkout

When the Logic and Memory Subsystem were combined, a step-by-step checkout procedure was established to insure proper performance of the read, clear-write, inhibit sense amplifier, and increment operations. The first part of the procedure was designed to insure a complete information path from the logic X register to the write register through digit drivers, read register and back to the X register (XR⟶ WR⟶ DD⟶ RR⟶ X). This proved to be successful, the memory was inhibited and continuity through the path was established.

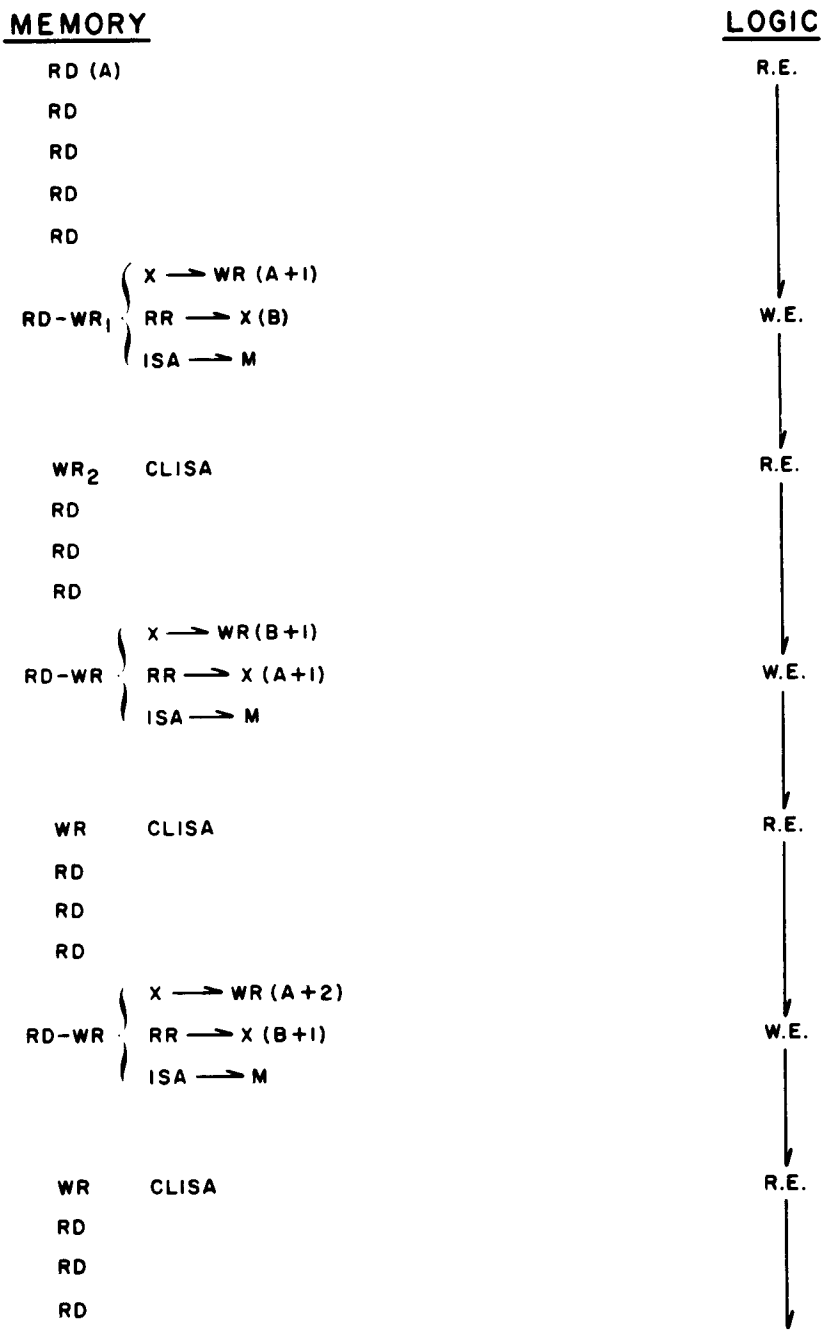


Figure 2-5. Timing Relationship Between Logic and Memory

It had been suspected that some difficulty would be encountered in obtaining time coincidence of the word write driver pulse and the digit driver pulse required to perform a write "1" on the clear-write cycle. This suspicion was confirmed when a write operation was attempted. An option was available because the digit driver pulse and the write driver pulse could both be varied in time by changing the WR⟶DD timing pulse (which clocks information out of the write register) or the D⟶YS timing pulse (which clocks the decoder Y outputs into the Y drivers). Since moving the WR⟶DD would also affect the information transfer loop, the alternative of moving the D⟶YS was chosen.

When the Logic and Memory Subsystem tables were moved together, three feet of space was left to allow access to both tables. This additional distance caused the information from the X register to arrive late at the write register. To compensate for this delay, WR⟶DD was delayed allowing the information to arrive at the write register before it was clocked out.

The difficulty encountered when trying to write into a memory word and then read the information out was previously described in Section A, Review. Essentially the logic was trying to read information out of memory which was written-in about 5 nanoseconds before. As a result, information was passing from the write register to the digit drivers and directly to the read register, where the logic retrieved it. Thus the storage of information in memory cells was bypassed. To correct the situation several timing pulses were changed:

(a) WR (timing pulse which initiates a clear-write cycle in memory) was delayed so it would have no effect during the read cycle. Information was transferred from the X register to the write register for temporary storage. To do this WR was delayed such that WR⟶DD had already occurred but not too close to RD (initiates transfer from memory read register to the logic X register). This was necessary since 10 nanoseconds is required to clear the X register before a transfer in from memory.

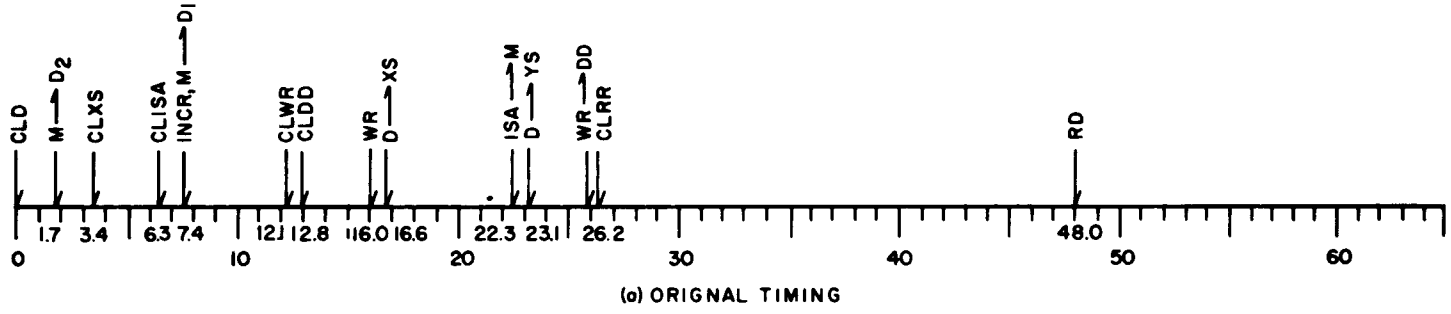
(b) ISA⟶M (clocks the inhibit sense amplifier circuits) was delayed until the read-regenerate cycle is completed so that the inhibit is on for the next cycle where clear-write occurs.

(c) ISA (enables the inhibit sense amplifier) level from logic was delayed to provide time coincidence with ISA — M at the inhibit sense amplifier AND gate.

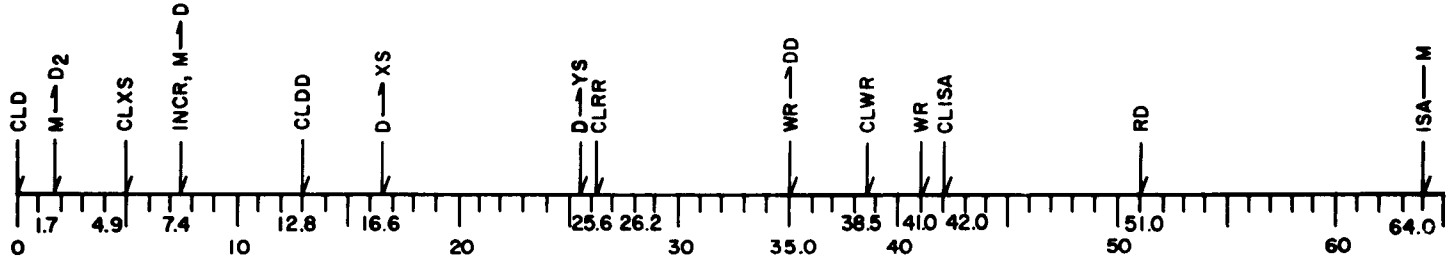
(d) The write register had to be cleared after a transfer to the digit driver (WR⟶DD) and before a transfer into the write register from the logic (WR).

(e) The inhibit sense amplifier driver must be cleared prior to use. Therefore, CLISA (Clear Inhibit Sense Amplifier) was delayed until it preceded ISA⟶M by approximately 16 nanoseconds allowing inhibit sense amplifier recovery and sufficient clear pulse width.

Figure 2-6 shows the timing as originally proposed and as it now exists in the subsystem with all modifications required to obtain satisfactory operation.



(a) ORIGNAL TIMING



(b) REVISED TIMING

Figure 2-6. Details of Subsystem Timing

2. Circuits

a. General

For the combined functioning, it was necessary to operate the read-write register and the inhibit sense amplifier as well as maintain the performance of previously operating circuits such as the counter, decoder, X and Y drivers, and the memory stack with its peripheral circuitry (sense amplifiers, digit drivers and word drivers).

b. Counter and Decoder

The counter and decoder would have required little maintenance but for numerous connection failures at the wafers and some at the Hi-K power line screws. The wafer connections were usually re-established by manual manipulation of the wafers themselves without removal. The power lines were repaired by tightening the nuts on the screws. About 5 or 6 wafers had to be removed for repairs which involved replacement of two diodes, one resistor and resoldering.

c. X and Y Drivers

The X and Y drivers required no maintenance once the original debugging was completed, however the tolerance on the Y power supply has become more critical since the additional circuitry was added. This is because the Y driver can change the coincidence of the write and digit driver pulses used in the clear-write cycle.

d. Memory Stack

Before as well as during the combined operation and debugging, the memory was periodically checked for its capability to recycle "1"s and "0"s while sequencing all the words. Except for an intermittent failure of the entire fifth digit line on the second plane, this operation was not too difficult to maintain. Due to inaccessibility this condition was not diagnosed, however, 4 of the 5 locations were restored to operation when the tunnel rectifier was removed from the location at the eighth word. It was necessary to determine the sense amplifier current range and nominal operating point several times during this period to maintain this operation. It is not known at this time whether this "drift" was due to other bias changes mentioned above or due to actual component or diode drift. At least one of the 5% resistors in the sense amplifier bias circuit had to be changed because of drifting.

The above operation proved to be a minimum requirement for operation in combination with logic or even from the memory table console (using dynamic writing and inhibiting rather than static). For lack of time and because of accessibility, it was decided to try to achieve complete operation with the fourth plane only. This was achieved, but only after three diodes were changed on the fourth plane. These diodes had been operating satisfactorily with static writing and inhibiting and with good sense amplifier current range (± 2%). An operating range for the sense amplifier, digit driver, and memory cells power supplies had to be found for the more critical combined operation.

e. Inhibit Sense Amplifier

Both the inhibit sense amplifier and the read-write register were coupled to the sense amplifiers and digit drivers (respectively) by means of micro-dot connectors. This proved to be convenient, but lacked reliability especially when the leads were disturbed. However the chief problem with the inhibit sense amplifier was that the positive inhibiting pulses were differentiated into negative going pulses. These pulses were in some cases capable of firing the first and/or second stages of the sense amplifier and/or the first stage of the digit driver. This problem was expediently solved by attenuating the inhibiting pulse to an amplitude just necessary to inhibit the sense amplifier and by reducing the bias at the power supplies. Inhibiting was also hampered by the fact that the planes (second & fourth) with the preamps are more readily inhibited at the preamp than at the first or second stage of the sense amplifier. This is believed to be due to the reduction of the effective read pulse by the firing of the preamp while the second stage is being inhibited. Thus the read pulse does not have sufficient effective amplitude to switch the memory cell to the high "0" state when the preamp fires. This switching was assisted by reducing the load on the word lines due to the oscilloscope "look-ins", by raising the memory cell bias, and by lowering the bias on the digit lines.

f. Read-Write Register

Although the read-write register was checked out before installing and coupling it to the memory stack, numerous troubles (besides micro-dot connectors and timing problems discussed elsewhere in this report) showed up or developed at this time. The 16.3-ma diode on a WBA (Write-Bistable-AND-Wafer) had to be replaced because the peak was too high. Three OR diodes had to be replaced because of shorts or opens. At one location no WBA wafer would reset. Rather than investigate the location, which would have taken considerable time, the reset pulse was increased by raising the inductance on the AI (AND-Inhibit) wafer. It was not discovered until later that the inductance was increased so much that the AI had trouble recovering in one cycle. However, this did not cause any error in the programmed exercises since the memory cycles five times to each one of logic. After coupling the read-write register to the digit drivers, the three digit driver power supplies had to be changed to compensate for the current drawn through the coupling lines.

C. EXTENSIBILITY MEMORY

1. General

The extensibility plane, consisting of two 24-bit words, was mounted on the frame of the nine-word memory subsystem. Since the nine-word subsystem has only three regeneration loops, only three of the 24 digits on the extensibility plane could be regenerated. The worst-case positions (the two ends of the word lines) were chosen and the middle digit was used for regeneration. To simulate 24-bit operation from the word drive point of view, all digit lines not being sensed and regenerated were loaded with 25-ohm resistors to simulate loading of sense amplifier-digit driver combinations.

2. Testing

The main difficulty encountered in achieving operation of the extensibility plane was in insuring coincidence between the digit and write pulses. The sense amplifiers and digit drivers of the system had been speeded up to the point where the digit pulse was occurring much too early for coincidence with the write pulse. The problem could have been solved by adding delay in the regeneration loops. However, since it was desired to maintain operation of the original memory plane of the system, this wasn't done. The reason for lack of coincidence was that the read and write pulses on the extensibility plane were much wider than on the three-word three-bit plane. Since the pulses were wider, the spacing between them was longer and the write pulse occurred too late. By decreasing the inductance in the read driver circuit, its output pulse was made narrower and consequently the spacing between read and write was shortened. With this modification the three regeneration digits were put into operation.

To test the other digits on the extensibility plane, the memory cell bias was inhibited, bringing all the cells to their low "1" state. A single input pulse was then applied to the word read driver. By measuring the state of each memory cell with a high-impedance voltmeter it was found that all cells were driven to their high state. This showed that worst-case bit storage (all "1"s) could be read.

At present, the extensibility plane has been in operation for more than a month with the only failure being due to a drift in bias of one of the word driver circuits. The repetition rate of the regeneration loop is 65 megacycles and the sense amplifiers are recovering in less than 8 nanoseconds.